AMENDMENTS

IN THE SPECIFICATION:

Please replace the first paragraph on page 11 with the following amended paragraph:

In a typical application, the suspend mode of operation requires that the voltage applied to the VDDA input be kept at a normal voltage level (*e.g.*, about 1.0 to 1.3V) while the array nwell supply input (VNWA) be raised to a higher voltage level (*e.g.*, 1.8V). The RET signal raises from about 0V to a normal voltage level (*e.g.*, about 1.0 to 1.3V) and the RETB signal drops from a normal voltage level to about 0V. The VSSA input and word line rise to the sinking suspend voltage generated by the sinking voltage regulator 306 (*e.g.*, about 0.3 to 0.8V or 0.7 to 0.4 V below the normal mode voltage). A bit line (BL) typically floats to a voltage level close to the suspend voltage. One or more additional gate-sinking voltage keeper components can also be employed that controllably connect bit lines of the memory array 314 to the sinking suspend voltage regulator 306.

Please replace the last paragraph on page 10 and continuing on to page 11 with the following amended paragraph:

The sinking voltage regulator 306 generates and supplies the sinking suspend voltage at least during the suspend mode of operation. The sinking suspend voltage is supplied to the first gate-sinking voltage keeper component 308 and the second gate-sinking voltage keeper component 310 such that the memory array 314 can receive the sinking suspend voltage during the suspend mode of operation. Additionally, the sinking voltage regulator 306 can operate to sink leakage current generated by the memory array 314. Furthermore, the sinking voltage regulator 306 can be a low-dropout voltage regulator (LDO).